REMARKS

Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

At the outset, the Applicants wish to thank the examiners for the courtesy shown to their representatives during a personal interview on June 21, 2005 and during telephone interviews on July 15 and 19, 2005. During these interviews, it was agreed that the above claim amendments would render the claims allowable over the applied art of record.

The following includes a summary of the substance of the interviews.

This amendment revises independent claims 19 and 27 for clarity and to highlight patentable aspects of this invention. Claims 21 and 29 are also clarified. It is noted that the Amendment filed November 22, 2004 was not entered. The subject matter of the new claims is supported at least at application page 8, line 21-page 9, line 17, and page 17, line 21-page 19, line 21, and in Fig. 3 and Fig. 5.

In the office action of March 29, 2005, claims 19-30 were rejected under 35 USC 103(a) as unpatentable over Bussgang.

Claims 19 and 27 recite features of:

(1) a first information sequence comprising a plurality of bits in series,

(2) a second information sequence comprising a plurality of bits in series,

(3) these sequences are input through different routes,

(4) the first information sequence is more important than the second information sequence,

(5) generation of a sequence of bits including at least one bit of the first information sequence and at least one bit of the second information sequence, and

(5) modulation of the sequence of bits wherein a bit corresponding to the first information sequence is arranged on the first bit of each symbol of the sequence of bits.

In contrast, Bussgang discloses:

(1) only a single analog signal input that is A/D converted to a sequence comprising a plurality of bits,

(2) series-to-parallel conversion of the sequence of bits,

(3) parallel-to-series conversion (elements 12, 13, 14) of the bits, and

(4) converting the parallel bits such that the two high order bits are in the first bit position in the two formed symbols.

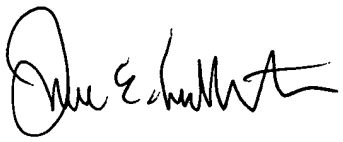
Bussgang does not teach or suggest at least the above-noted claimed subject matter. It is particularly noted that Bussgang fails to teach or suggest inputting of first and second information sequences each comprising a sequence of a plurality of bits in

series. Instead, in Bussgang, the inputted information is a single analog signal, that is digitized and converted to parallel data, and single bits are input in parallel to the converter 12, 13, 14. Thus, in Bussgang, the inputted information are parallel bits. From the above, it is apparent that the overall concept, structure and operation of the present claimed invention is quite different from, and patentably distinguishes over, Bussgang.

For at least the above reasons, and as agreed during the interviews, the present claims are allowable over the teachings of Bussgang et al. Therefore, a notice of allowance is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



Date: July 21, 2005

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